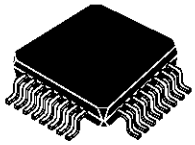
SGS-THOMSON MICROELECTRONICS

L4992

TRIPLE OUTPUT POWER SUPPLY CONTROLLER

PRODUCT PREVIEW

- DUAL PWM BUCK CONTROLLERS (3.3V and 5.1V)
- 12V/120mA LINEAR REGULATOR
- DUAL SYNCH RECTIFIERS DRIVERS
- 96% EFFICIENCY ACHIEVABLE
- 50µA @ 12V IN STAND BY
- 5.5V TO 20V SUPPLY VOLTAGE
- EXCELLENT LOAD TRANSIENT RESPONSE
- DISABLED PULSE SKIPPING FUNCTION
- POWER MANAGEMENT:
  - UNDER AND OVERVOLTAGE OUTPUT DETECTION
  - POWER GOOD SIGNAL
  - SEPARATED DISABLE
- HYSTERESIS THERMAL SHUTDOWN
- PACKAGE: TQFP32 PIN



TQFP32

ORDERING NUMBER: L4992

APPLICATION

- NOTEBOOK AND SUBNOTEBOOK COMPUTERS
- PEN TOP AND PORTABLE EQUIPMENT
- COMMUNICATING COMPUTERS

DESCRIPTION

The L4992 is a sophisticated dual PWM step-down controller and power monitor intended for Notebook computer and/or battery powered equipment. The device produces regulated +3.3V, +5.1V and 12V supplies for use in portable and PCMCIA applications.

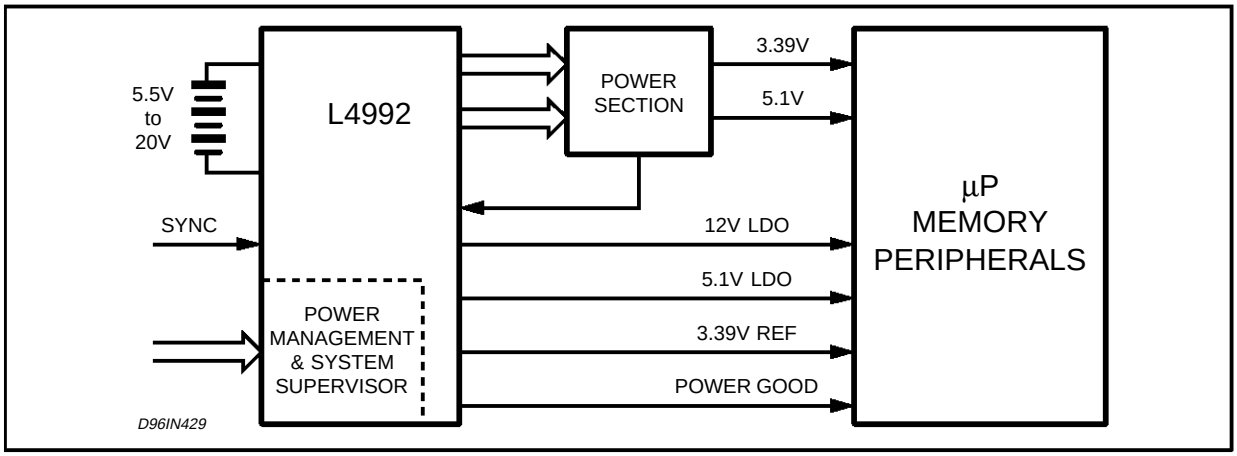
The internal architecture allows to operate with minimum external components count. A very high switching frequency (200/300 KHz or externally synchronizable) optimizes their physical dimensions.

Synchronous rectification and pulse skipping mode for the buck sections optimise the overall efficiency over a wide load current range (96% efficiency @1A/5.1V and 93% efficiency @ 0.05A/5.1V.

The two high performance PWM controllers for +3.3V and +5.1V lines are monitored for overvoltage, undervoltage and overcurrent conditions. On detection of a fault a POWER GOOD signal is generated and a specific shutdown procedure takes place to prevent physical damage and data corruption.

A disable function allows to manage the output power sections separately, optimising the quiescent consumption of the IC in stand-by conditions.

SYSTEM BLOCK DIAGRAM



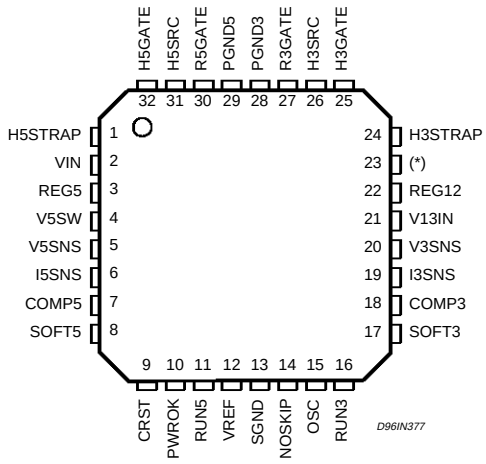
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	Power Supply Voltage on V_{IN}	0 to 25	V
V_I	Maximum Pin Voltage to Pins 1, 24, 25, 32	-0.5 to (V_{IN} +5)	V
I_{IN}	Input Current Except V13IN and V_{IN}	-1 to +1	mA
I_{OUT}	Output Current Digital Output	-15 to +15	mA
T_J	Junction Temperature	-55 to 150	°C

THERMAL DATA

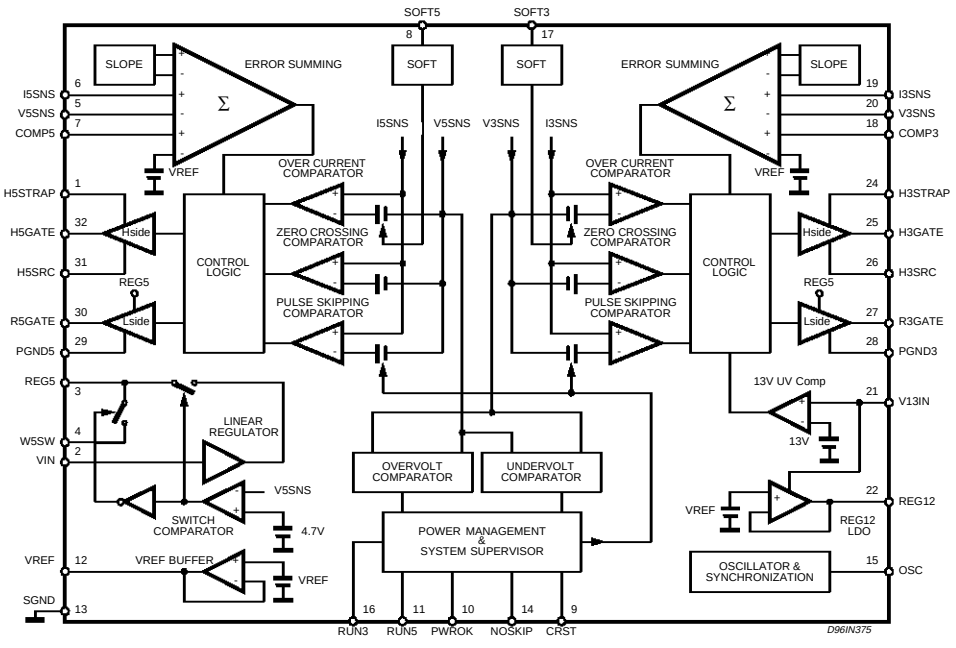
Symbol	Parameter	Value	Unit
$R_{TH\ J\text{-}amb}$	Thermal Resistance Junction -Ambient	60	°C/W

PIN CONNECTION (Top view)



(*)TO BE CONNECTED TO PIN13

BLOCK DIAGRAM



PIN FUNCTIONS

N.	Name	Description
1	H5STRAP	+5.1V section bootstrap capacitor connection
2	V_{IN}	Device supply voltage. From 5.5 to 20V
3	REG5	+5V regulator supply. Used mainly for bootstrap capacitors. It should be bypassed to ground.
4	V5SW	Alternative device supply voltage. When the +5.1V section is operating, the device is no longer powered through V_{IN} but through this pin.
5	V5SNS	This pin connects to the (-) input of the +5.1V internal current sense comparator
6	I5SNS	This pin connects to the (+) input of the +5.1V internal current sense comparator
7	COMP5	Feedback input for the +5.1V section.
8	SOFT5	Soft-start input of the +5.1V section. The soft-start time is programmed by an external capacitor connected between this pin and SGND. Approximately, 1ms/nF @ full load.
9	CRST	Input used for start-up and shut-down timing. A capacitor defines a time of 2ms/nF.
10	PWROK	Power-good diagnostic signal. This output is driven high when both switching sections are enabled and running properly, after a delay defined by the CRST capacitor.
11	RUN5	Control input to enable/disable the 5.1V section. A high level (>2.4V) enables this section, a low level (<0.8V) shuts it down
12	VREF	Internal +3.39V high accuracy voltage generator. It can source 5mA to external load. Bypass to ground with a 4.7µF capacitor to reduce noise.
13	SGND	Signal ground. Reference for internal logic circuitry. It must be routed separately from high current returns.
14	NOSKIP	Pulse skipping mode control. A high level (>2.4V) disables pulse skipping at low load current, a low level (<0.8V) enables it.
15	OSC	Oscillator frequency control: connect to 2.5V to select 300KHz operation, to ground or to 5V for 200KHz operation. A proper external signal can synchronize the oscillator
16	RUN3	Control input to enable/disable the +3.3V section. A high level (>2.4V) enables this section, a low level (>0.8V) shuts it down.
17	SOFT3	Soft-start input for the 3.3V section. The soft-start time is programmed by an external capacitor connected between this pin and GND. Approximately, 1ms/nF @full load.
18	COMP3	Feedback input for the +3.3V section
19	I3SNS	This pin connects to the (+) input of the +3.3V internal current sense comparator
20	V3SNS	This pin connects to the (-) input of the +3.3V internal current sense comparator
21	V13IN	12V regulator input supply voltage, included between 13 and 20V. This voltage can be supplied by a flyback winding on +3.3V inductor
22	REG12	12V regulator output voltage. It can source up to 150mA to an external load
23	SGND	To be connected to pin 13
24	H3STRAP	+3.3V section bootstrap capacitor connection
25	H3GATE	Gate- driver output for the +3.3V high-side N-MOS
26	H3SRC	+3.3V high-side N-MOS source connection
27	R3GATE	Gate- driver output for the +3.3V low- side N-MOS (synchronous rectifier).
28	PGND3	Current return for +3.3V section drivers
29	PGND5	Current return for +5.1V section drivers
30	R5GATE	Gate-driver output for the +5.1V low-side N-MOS (synchronous rectifier).
31	H5SRC	+5.1V high-side N-MOS source connection
32	H5GATE	Gate-driver output for the +5.1V high-side N-MOS

ELECTRICAL CHARACTERISTICS (V_{IN} = 12V; T_J = 25°C; V_{OSC} = GND; unless otherwise specified.)

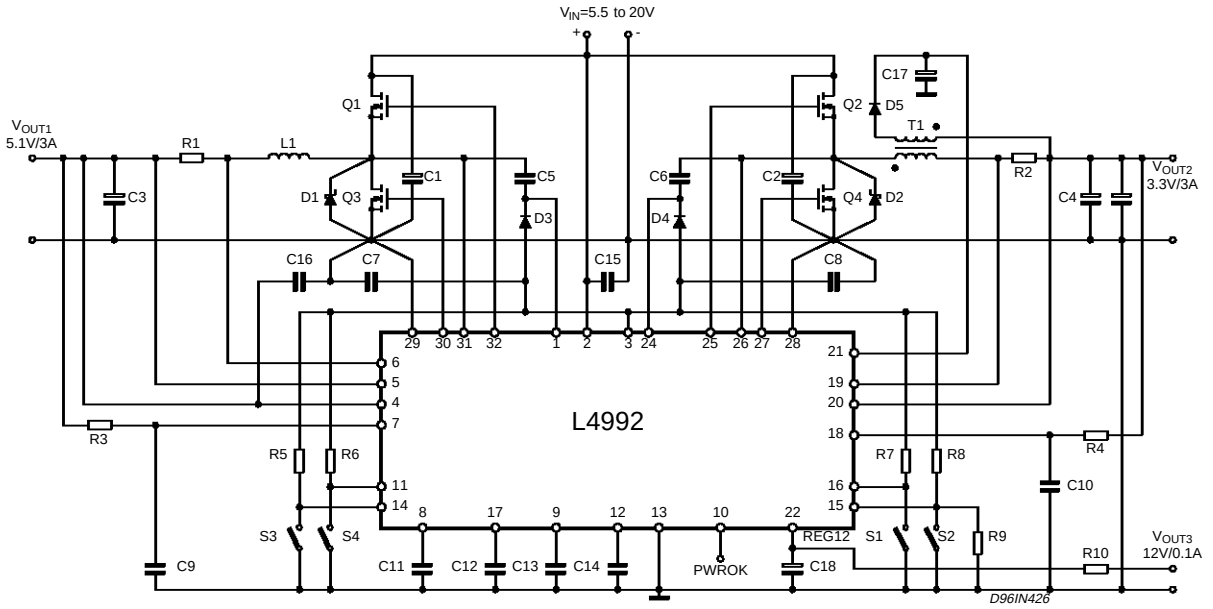
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
V_{IN}	Input Supply Voltage		5.5		20	V
I_2	Operating Quiescent Current	R5GATE = R3GATE = OPEN H5GATE = H3GATE = OPEN RUN3 = RUN5 = REG5 (DRIVERS OFF)			1.35	mA
I_2	Stand-By Current	RUN3 = RUN5 = GND V_{IN} = 12V V_{IN} = 20V		50 60	100 120	µA
+5.1V PWM CONTROLLER SECTION						
V_{5OUT} (*)	V5SNS Feedback Voltage	V_{IN} = 5.5 to 20V; V_{I5SNS} - V_{V5SNS} = 0 to 70mV	4.975	5.13	5.285	V
V_6 - V_5	Over-Current Threshold Voltage	VSOFT5 = 4V	80	100	120	mV
V_6 - V_5	Pulse Skipping Mode Thereshold Voltage	V_{IN} > 6.8V	18	28	38	mV
		V_{IN} < 5.8V	7	13	19	mV
V_5	Over Voltage Threshold ON V5SNS		5.35	5.55	5.77	V
	Under Voltage Threshold ON V5SNS		4.54	4.69	4.87	V
+3.3V PWM CONTROLLER SECTION						
V_{3OUT} (*)	V3SNS Feedback Voltage	V_{IN} = 5.5 to 20V; V_{I3SNS} - V_{V3SNS} = 0 to 70mV	3.285	3.39	3.495	V
V_{19} - V_{20}	Over Current Threshold Voltage	VSOFT3 = 4V	80	100	120	mV
V_{19} - V_{20}	Pulse Skipping Mode Threshold Voltage	V_{IN} = 5.5 to 20V;	18	28	38	mV
V_{20}	Over Voltage Threshold ON V3SNS		3.55	3.7	3.85	V
	Under Voltage Threshold ON V3SNS		3.02	3.14	3.27	V
PWM CONTROLLERS CHARACTERISTICS (BOTH SECTIONS)						
F_{OSC}	Switching Frequency Accuracy	OSC = REG5/2	255	300	345	kHz
		OSC = 0 or REG5	170	200	230	kHz
V_{15}	Voltage Range for 300kHz Operation		2.4		2.6	V
T_{OFF}	Dead Time		300	375	450	ns
T_{OV}	Overvoltage Propagation Time	V5SNS to PWROK or V3SNS to PWROK			1.25	µs
T_{UV}	Undervoltage Propagation Time	V5SNS to PWROK or V3SNS to PWROK			1.5	µs
I_8, I_{17}	Soft Start Charge Current		3.2	4	4.8	µA
V_8, V_{17}	Soft Start Clamp Voltage			4		V

(*) Guaranteed by design, not tested in production

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
HIGH AND LOW SIDE GATE DRIVER (BOTH SECTIONS)						
I_{25}, I_{27}, I_{32}, I_{30}	Source Output Peak Current	C_{LOAD} = 1nF	0.2	0.5		A
	Sink Output Peak Current	C_{LOAD} = 1nF	0.2	0.5		A
R_H	R_{DSON} Resistance (or Impedance)	Driver OUT HIGH			7	Ω
R_L	R_{DSON} resistance (or Impedance)	Driver OUT LOW			5	Ω
V_{OH}	Output High Voltage	HSTRAP = REG5 I_{SOURCE} = 10mA; HSRC = GND	4.40	5.3	5.61	V
V_{OL}	Output Low Voltage	HSTRAP = REG5 I_{SINK} = 10mA HSRC = GND			0.5	V
T_{CC}	Cross-Conduction Delay		30	75	130	ns
12V LINEAR REGULATOR SECTION						
V_{21}	Input Voltage Range		13		20	V
V_{22}	Output Voltage	I_{22} = 0 to 120mA	11.54	12.0	12.48	V
I_{22}	Current Limiting	V_{REG12} = 12V	120			mA
	Short Circuit Current	V_{REG12} = 0V	150			mA
V_{CP}	Input Voltage Clamp	I_{CLAMP} = 100µA	16			V
	”One Shot” Activation Threshold	V_{13IN} Falling	12.88	13.7	14.52	V
	”One Shot” Pulse				1.5	µs
INTERNAL REGULATOR (VREG5) AND REFERENCE VOLTAGE						
V_3	VREG5 Output Voltage	V_{IN} = 5.5 to 20V I_{LOAD} = 0 to 5mA	4.5	5.3	5.61	V
I_3	Total Current Capability	V_{REG5} = 5.3V V_{REG5} = 6V	25 70			mA
	Switch-Over Threshold Voltage		4.37	4.53	4.7	V
V_{12}	Reference Voltage		3.35	3.39	3.43	V
		V_{IN} = 5.5 to 20V I_{LOAD} = 1 to 5mA	3.32	3.39	3.46	V
I_{12}	Source Current at Reference Voltage		5			mA
POWER GOOD AND ENABLE FUNCTION						
V_{16}, V_{11}	RUN3, RUN5, Enable Voltage	HIGH LEVEL	2.4			V
V_{16}, V_{11}	RUN3, RUN5, Disable Voltage	LOW LEVEL			0.8	V
T_{10}	Power Good Delay	C_{CRST} = 100nF	160	200	240	ms
T_{27}, T_{30}	Shutdown Delay Time before Low Side Activation (Except Over-Voltage Fault)	C_{CRST} = 100nF,	160	200	240	ms
	CRST Timing Rate			2		ms/nF
	Power Good High Level	I_{pwROK} = 40µA	4.1			V
	Power Good LowLevel	I_{pwROK} = 320µA			0.4	V
SYNC						
	Synchronisation Pulse Width		400			ns
	Synchronisation Input Voltage (Falling Edge Transition)		5			V

Figure 1: Evaluation Board Circuit



R1 = 25mΩ, 1%, 0.5W
R2 = 20mΩ, 1%, 0.5W
R3,R4 = 270Ω, 1%
R5,R6,R7,R8,R9 = 1MΩ
R10 = 0.5Ω
N.B. All parts are SMD; the precision is 5% and the power rating is 1/8W, unless otherwise specified.

S1,S2,S3,S4 = Quad DIP switch

C1,C2 = 100µF, 20V, SANYO OS-CON, p.n. 20SA100K
C3,C4 = 220µF 10V, SANYO OS-CON, p.n. 10SA220K
C5,C6 = 100nF
C7,C8,C15,C16 = 1µF
C14,C18 = 4.7µF
C17 = 15µF, 25V, SANYO OS-CON, p.n. 25SC15M
N.B. All parts are SMD; unless otherwise specified, ceramic or plastic.

IC = L4992 (TWINS), ST (TQFP32 package)

L1 = 10µH, 2.65A, SUMIDA, p.n. CDR125-100
T1 = 10µH, 3A, 1:4 transformer, TRANSPOWER, p.n. TTI5902

Q1,Q2,Q3,Q4 = Si9410DY, (SO-8 package)

D1,D2 = TMBYV10-40, ST (MELF case)
D3,D4 = TMMBAT46, ST (MINIMELF case)
D5 = SMBYW01-200, ST (SOD6 case)

DEMO BOARD-EVALUATION

Figure 2: Demo Board Efficiency vs Output Current

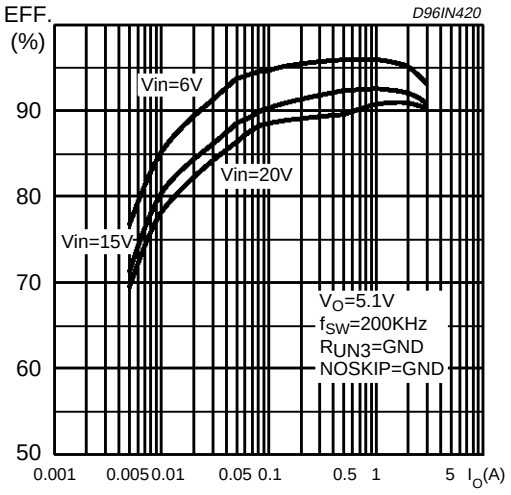


Figure 3: Demo Board Efficiency vs Output Current

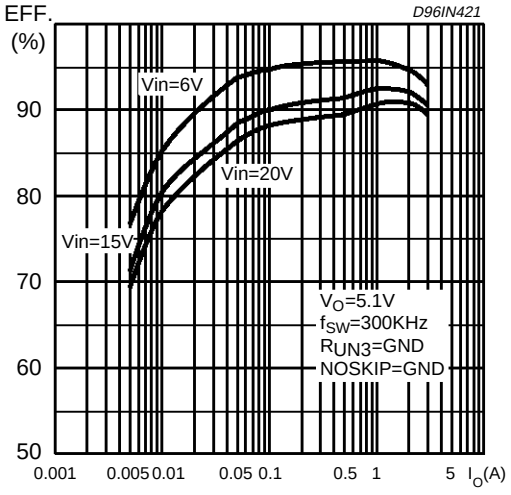


Figure 4: Demo Board Efficiency vs Output Current

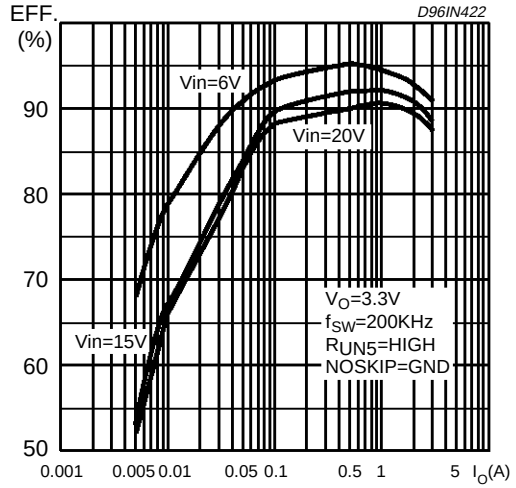


Figure 5: Demo Board Efficiency vs Output Current

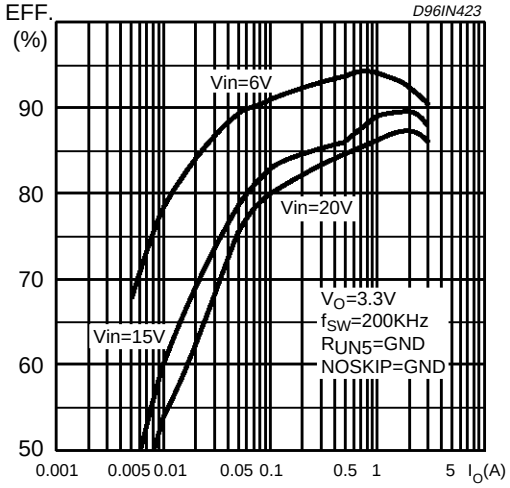


Figure 6: Switching Frequency vs Output Current (pulse skipping)

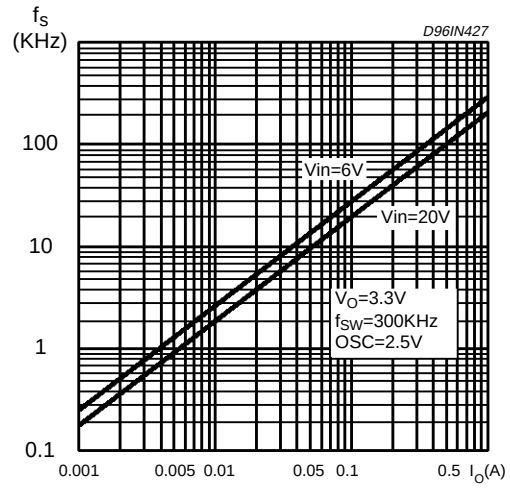
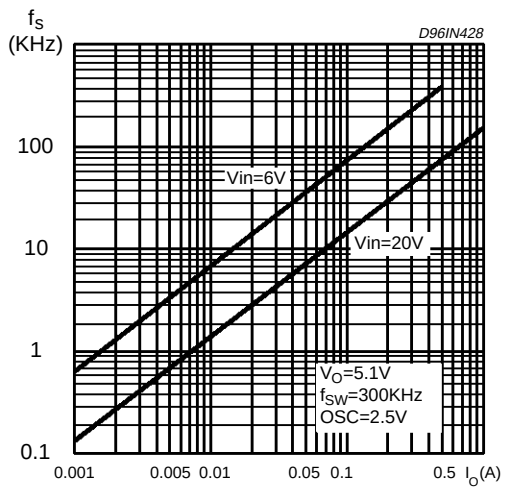


Figure 7: Switching Frequency vs Output Current (pulse skipping)



TQFP32 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.60			0.220	
e		0.80			0.031	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.60			0.220	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 7°(max.)